

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	24495	(prefetch\$3 or pre-fetch\$3 or ((look\$3 or read\$3) adj2 ahead))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:23
L2	852	(adaptive or variable or throttI\$3) with l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:23
L3	1561	711/137	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:25
L4	107	l2 and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:26
L5	94	l4 and @ad<"20030701"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:31
L6	19	bandwidth with l2 with l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:31
L7	277	l1 with depth	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:31
L8	31572	"711"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:31

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L9	86	I7 and I8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:31
L10	78	I9 and @ad<"20030701"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:44
L11	13012	(memory or storage) near2 utilization	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:33
L12	9	I1 same I2 same I11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:34
L13	6	(adjust\$3 or chang\$3 or var\$3) with I1 with I11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 14:18
L14	4	"6742102".pn. or "6542982".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:37
L15	6	("20040221111" "6233645" "6636945" "6687794" "6701316" "6742085").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/10/04 13:38
L16	10	aggressiv\$3 same moderat\$3 same I1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:40
L17	3	IOQ same I1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:43

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L18	96	(identif\$4 or detect\$3 or recogniz\$3) same l1 same depth	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:44
L19	69	l18 and @ad<"20030701"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:44
L20	23	l19 and bandwidth	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 13:48
L21	2	"6412046".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 14:17
L22	10706	(memory with response with (level or latency or delay))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 14:18
L23	77	l22 same l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 14:18
L24	14	(adjust\$3 or chang\$3 or var\$3) same l23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/10/04 14:19

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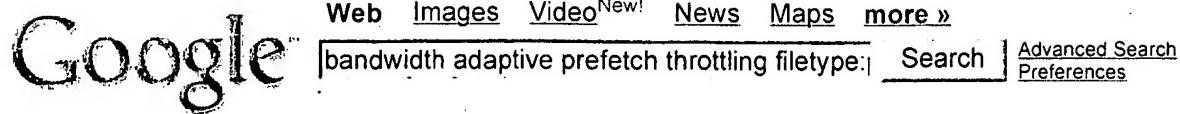
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#1	((prefetch* <paragraph> (throttl* <or> variable) <paragraph> adaptive)<in>metadata)	4
#2	((prefetch* <paragraph> thrott1*)<in>metadata)	1
#3	((prefetch* <sentence> adaptive)<in>metadata)	45

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- 1** [Tolerating memory latency through push prefetching for pointer-intensive applications](#)
- Chia-Lin Yang, Alvin R. Lebeck, Hung-Wei Tseng, Chien-Hao Lee
December 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**,
Volume 1 Issue 4

Publisher: ACM PressFull text available: [pdf\(590.24 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Prefetching is often used to overlap memory latency with computation for array-based applications. However, prefetching for pointer-intensive applications remains a challenge because of the irregular memory access pattern and pointer-chasing problem. In this paper, we proposed a cooperative hardware/software prefetching framework, the push architecture, which is designed specifically for linked data structures. The push architecture exploits program structure for future address generation instead ...

Keywords: Prefetch, linked data structures, memory hierarchy, pointer-chasing

- 2** [A study of integrated prefetching and caching strategies](#)
- Pei Cao, Edward W. Felten, Anna R. Karlin, Kai Li
May 1995 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1995 ACM SIGMETRICS joint international conference on Measurement and modeling of computer systems SIGMETRICS '95/PERFORMANCE '95**,
Volume 23 Issue 1

Publisher: ACM PressFull text available: [pdf\(1.25 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Prefetching and caching are effective techniques for improving the performance of file systems, but they have not been studied in an integrated fashion. This paper proposes four properties that optimal integrated strategies for prefetching and caching must satisfy, and then presents and studies two such integrated strategies, called *aggressive* and *conservative*. We prove that the performance of the *conservative* approach is within a factor of two of optimal and that the perfor ...

- 3** [Physical Experimentation with Prefetching Helper Threads on Intel's Hyper-Threaded Processors](#)

Dongkeun Kim, Steve Shih-wei Liao, Perry H. Wang, Juan del Cuívilo, Xinmin Tian, Xiang Zou, Hong Wang, Donald Yeung, Milind Girkar, John P. Shen

March 2004 **Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization CGO '04**

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